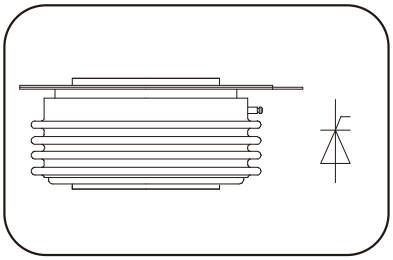
Phase Control Thyristors

G76KPC Phase Control Thyristors

Features

- Center amplifying gate
- Metal case with ceramic insulator
- Low on-state and switching losses

$I_{T(AV)}$	3500A
V_{DRM} / V_{RRM}	400~1000V
I_{TSM}	44 KA
I^2t	9680 10^3A^2S



Typical Applications

- AC controllers
- DC and AC motor control
- Controlled rectifiers

Symbol	Characteristic	Test Conditions	T_j(°C)	Value			Unit
				Min	Type	Max	
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Double side cooled T_{hs}=70°C	125			3500	A
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Double side cooled T_{hs}=55°C	125			4148	A
V_{DRM} V_{RRM}	Repetitive peak off-state voltage Repetitive peak reverse voltage	V_{DRM}&V_{RRM} tp=10ms V_{DSM}&V_{RSM}= V_{DRM}&V_{RRM}+100V	125	400		1000	V
I_{DRM} I_{RRM}	Repetitive peak current	V_{DM}= V_{DRM} V_{RM}= V_{RRM}	125			200	mA
I_{TSM}	Surge on-state current	10ms half sine wave V_R=0.6V_{RRM}	125			44	KA
I^2t	I^2t for fusing coordination					9680	A^2s*10^3
V_{TO}	Threshold voltage		125			0.82	V
r_T	On-state slop resistance					0.07	mΩ
V_{TM}	Peak on-state voltage	I_{TM}=5000A, F=40KN	25			1.80	V
dv/dt	Critical rate of rise of off-state voltage	V_{DM}=0.67 V_{DRM}	125			300	V/μs
di/dt	Critical rate of rise of on-state current	V_{DM}=67% V_{DRM} to 2000A,Gate pulse t_r ≤0.5μs I_{GM}=1.5A Repetitive	125			250	A/μs
I_{rm}	Reverse recovery current	I_{TM}=1500A,tp=1000 μs, di/dt=-20A/μs, V_R=50V	125			220	A
t_{rr}	Reverse recovery time					22	μs
Q_{rr}	Recovery charge					2420	μC
I_{GT}	Gate trigger current	V_A=12V, I_A=1A	25	40		300	mA
V_{GT}	Gate trigger voltage			0.8		3.0	V
I_H	Holding current			20		300	mA
V_{GD}	Non-trigger gate voltage	V_{DM}=67% V_{DRM}	125	0.3			V
$R_{th(j-h)}$	Thermal resistance Junction to heatsink	At 180° sine double side cooled Clamping force 40KN				0.011	°C/W
F_m	Mounting force			35		47	KN
T_{stg}	Stored temperature			-40		140	°C
W_t	Weight				1100		g
Outline	KT73cT						

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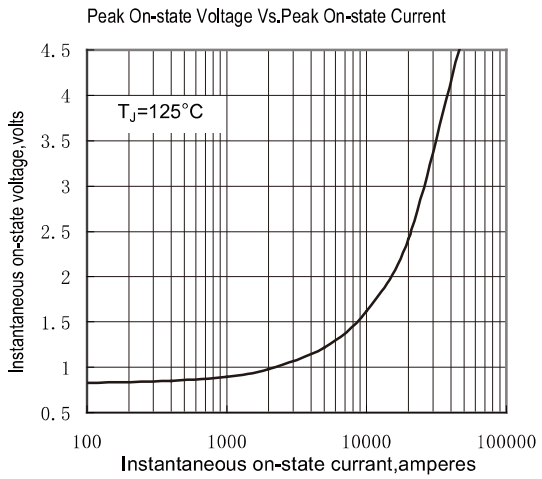

Fig.1

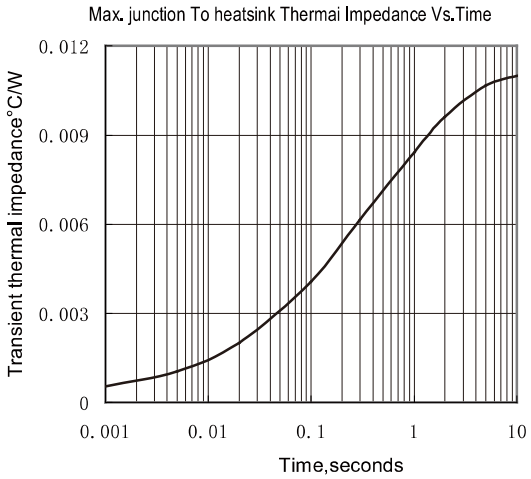

Fig.2

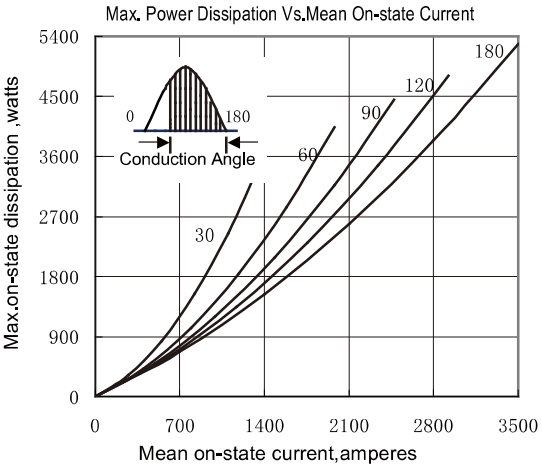

Fig.3

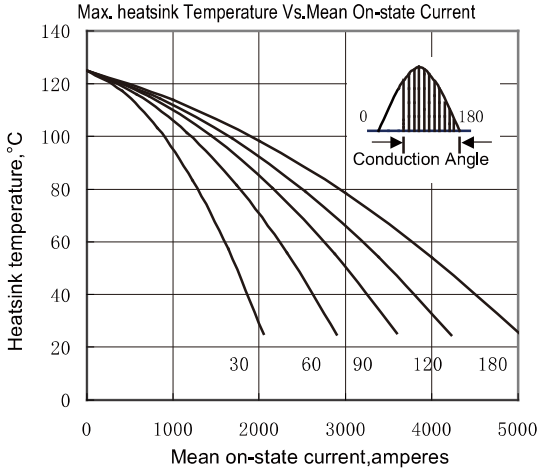

Fig.4

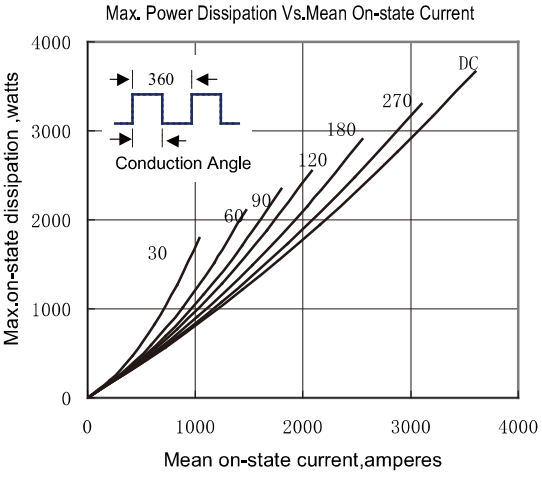

Fig.5

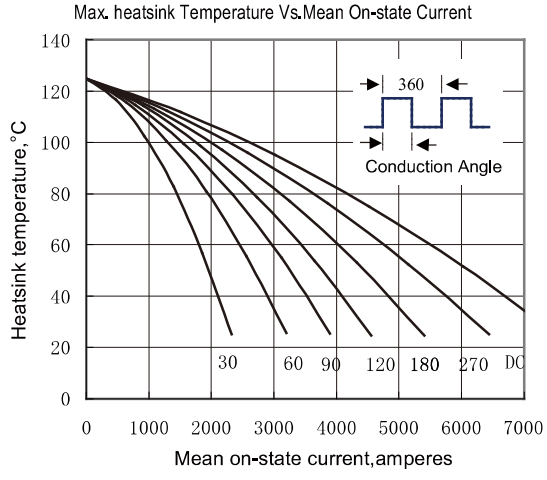

Fig.6

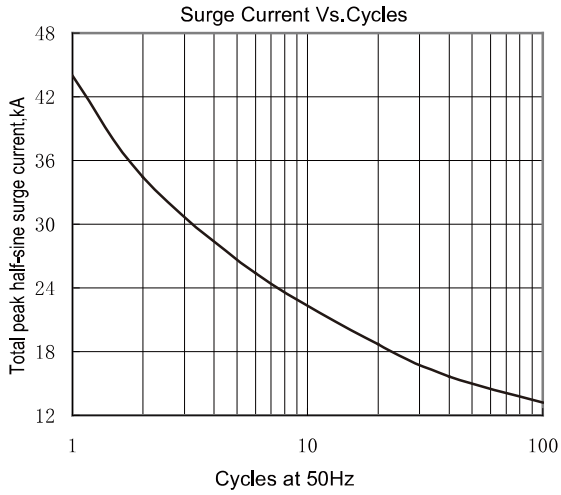

Fig.7

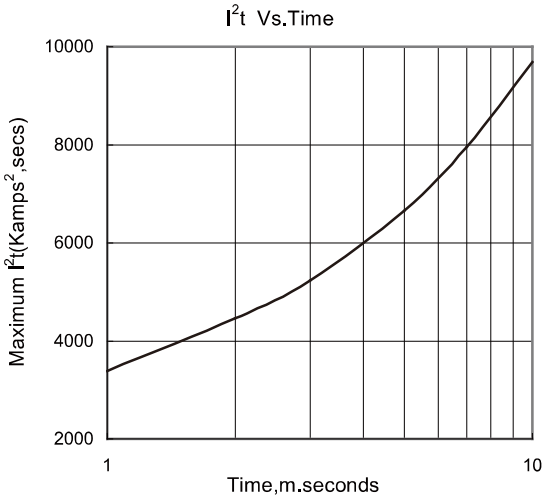

Fig.8

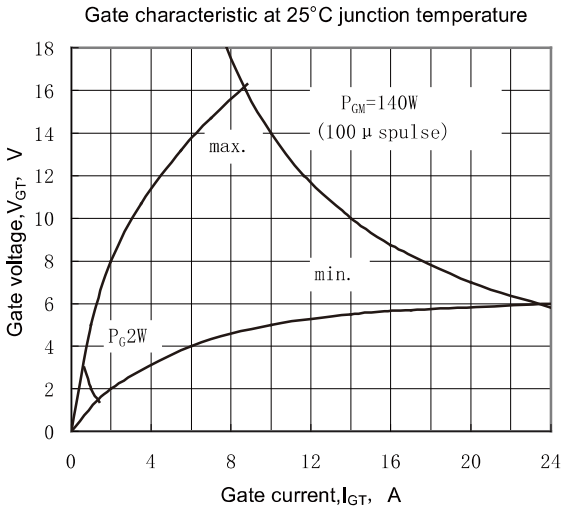

Fig.9

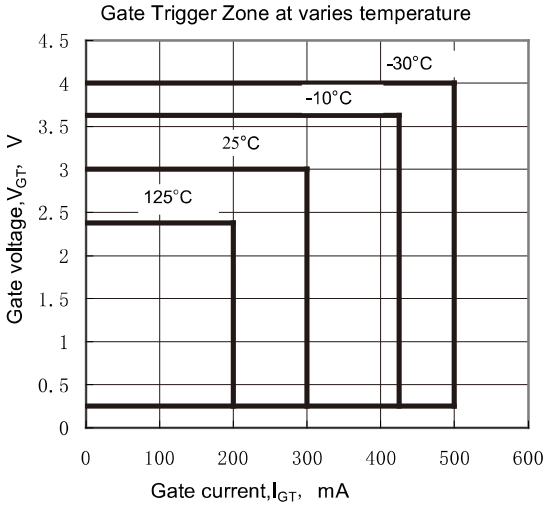

Fig.10

Outline: