

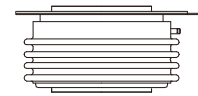
Features

- Center amplifying gate
- Metal case with ceramic insulator
- Low on-state and switching losses

Typical Applications

- AC controllers
- DC and AC motor control
- Controlled rectifiers

$I_{T(AV)}$	800A
V_{DRM} / V_{RRM}	3100~4200V
I_{TSM}	11.5 KA
I^2t	661 $10^3 A^2S$



Symbol	Characteristic	Test Conditions	$T_j(^{\circ}C)$	Value			Unit
				Min	Type	Max	
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Double side cooled $T_{hs}=70^{\circ}C$	125			800	A
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Double side cooled $T_{hs}=55^{\circ}C$	125			956	A
V_{DRM} V_{RRM}	Repetitive peak off-state voltage Repetitive peak reverse voltage	$V_{DRM} \& V_{RRM}$ $t_p=10ms$ $V_{DSM} \& V_{RSM} = V_{DRM} \& V_{RRM} + 100V$	125	3100		4200	V
I_{DRM} I_{RRM}	Repetitive peak current	$V_{DM} = V_{DRM}$ $V_{RM} = V_{RRM}$	125			100	mA
I_{TSM}	Surge on-state current	10ms half sine wave	125			11.5	KA
I^2t	I^2t for fusing coordination	$V_R = 0.6V_{RRM}$				661	$A^2s \cdot 10^3$
V_{TO}	Threshold voltage		125			1.24	V
r_T	On-state slop resistance					0.77	mΩ
V_{TM}	Peak on-state voltage	$I_{TM}=1500A, F=24KN$	25			2.8	V
dv/dt	Critical rate of rise of off-state voltage	$V_{DM}=0.67 V_{DRM}$	125			500	V/μs
di/dt	Critical rate of rise of on-state current	$V_{DM}=67\% V_{DRM}$ to 1500A, Gate pulse $t_r \leq 0.5\mu s$ $I_{GM}=1.5A$ Repetitive	125			100	A/μs
I_{rm}	Reverse recovery current	$I_{TM}=1000A, t_p=1000 \mu s,$ $di/dt=-20A/\mu s,$ $V_R=50V$	125			178	A
t_{rr}	Reverse recovery time					17.8	μs
Q_{rr}	Recovery charge					1588	μC
I_{GT}	Gate trigger current	$V_A=12V, I_A=1A$	25	40		300	mA
V_{GT}	Gate trigger voltage			0.8		3.0	V
I_H	Holding current			20		250	mA
V_{GD}	Non-trigger gate voltage	$V_{DM}=67\% V_{DRM}$	125	0.3			V
$R_{th(j-h)}$	Thermal resistance Junction to heatsink	At 180° sine double side cooled Clamping force 24KN				0.024	$^{\circ}C/W$
F_m	Mounting force			19		26	KN
T_{stg}	Stored temperature			-40		140	$^{\circ}C$
W_t	Weight				470		g
Outline	KT50cT						

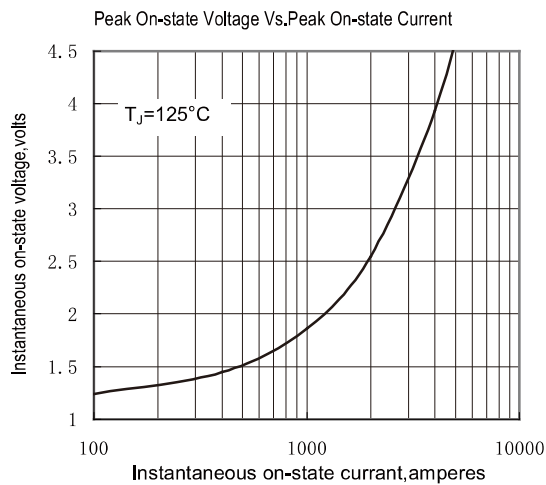


Fig.1

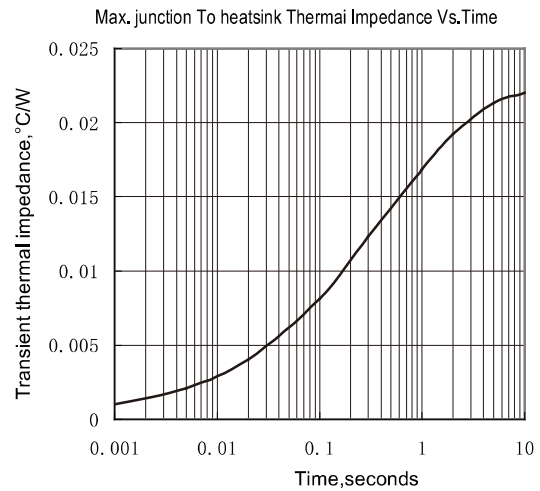


Fig.2

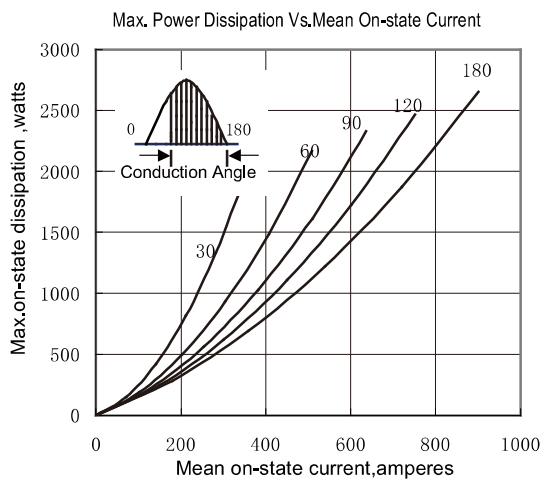


Fig.3

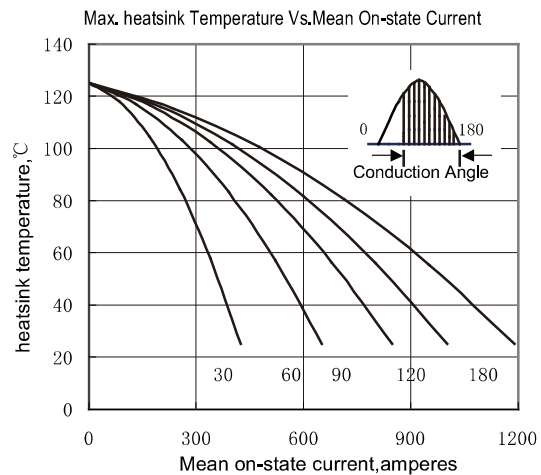


Fig.4

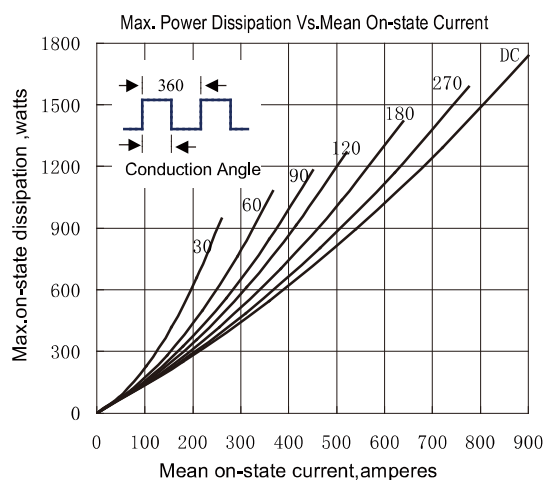


Fig.5

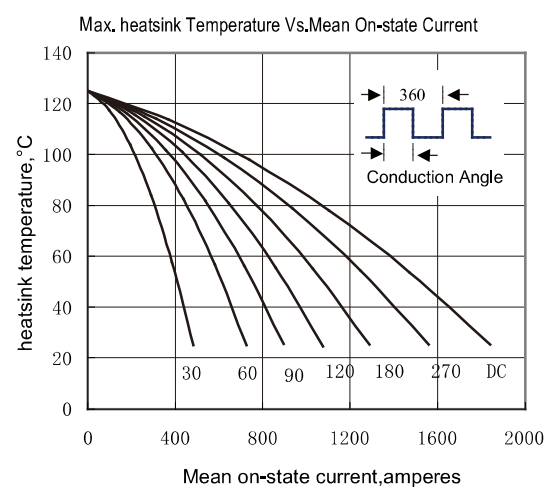


Fig.6

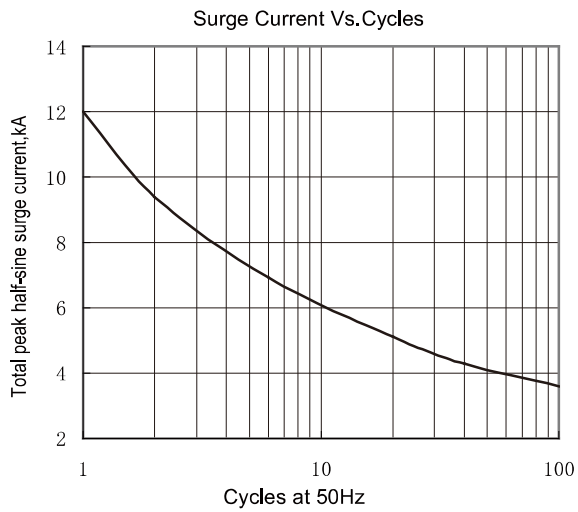


Fig.7

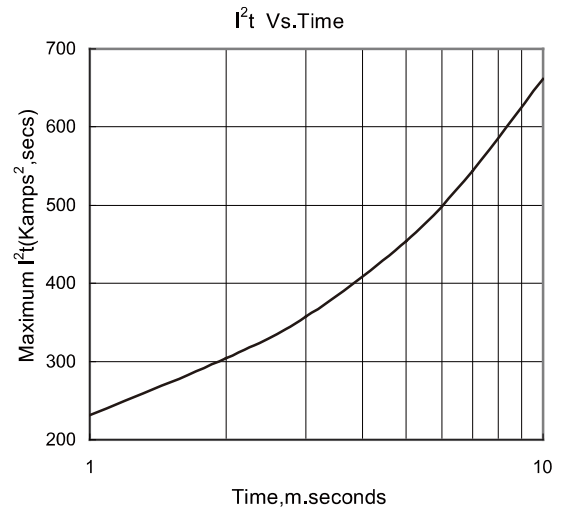


Fig.8

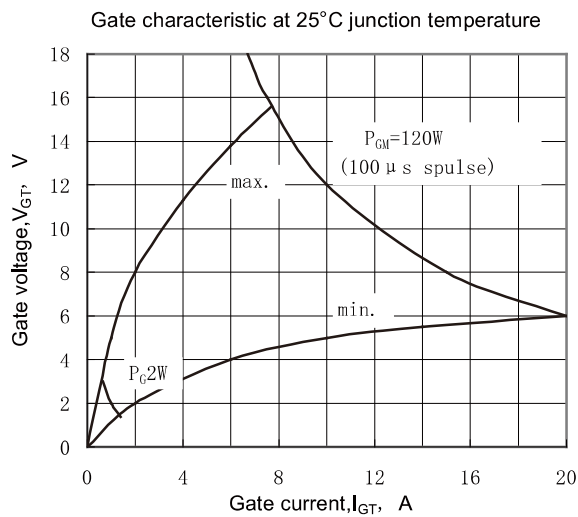


Fig.9

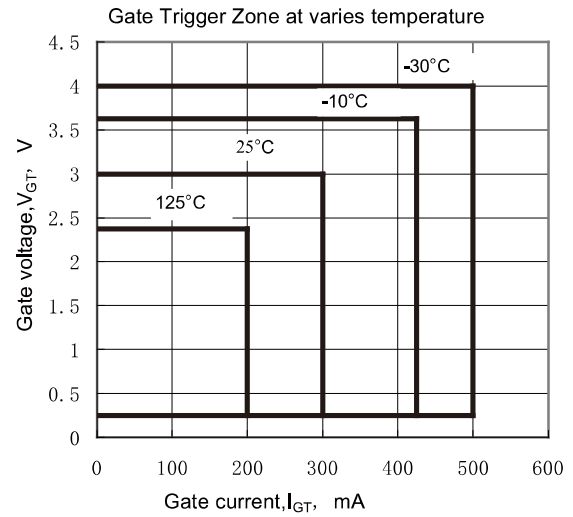


Fig.10

Outline:

