

T804 1400-20-24

Key Parameters

V_{DRM}	2000~2400	V
$I_{T(AV)}$	1470	A
I_{TSM}	23.0	kA
V_{TO}	0.96	V
r_T	0.23	mΩ

Applications

- SVC
- Motor drive
- Industry converter

Features

- Double-side cooling
- High power capability
- Low loss

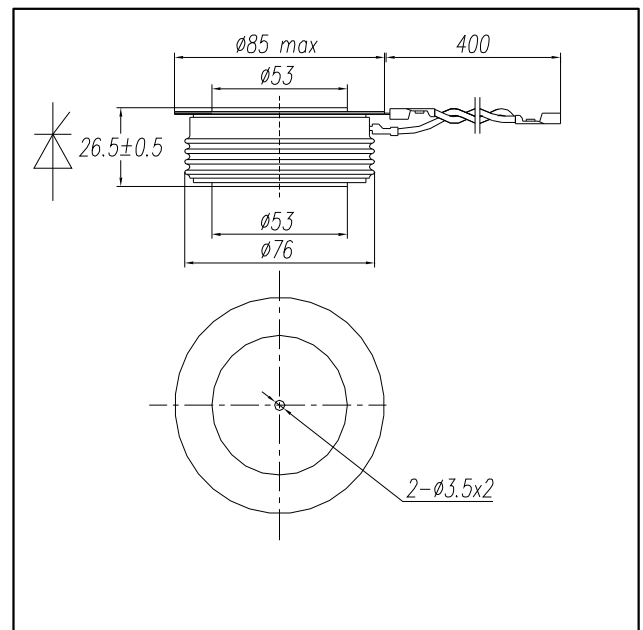
Thermal & Mechanical Data

Symb.	Parameter	Min	Type	Max	Unit
R_{thjc}	Thermal Resistance Junction to Case	-	-	0.018	K / W
R_{thcs}	Thermal Resistance Case to Heatsink	-	-	0.005	K / W
T_{vj}	Junction Temperature	-40	-	125	°C
T_{stg}	Storage Temperature	-40	-	140	°C
F	Mounting Force	-	30	-	kN
m	Weight	-	0.6	-	kg

Voltage Ratings

Device Type	$V_{DRM}/V_{RRM}(V)$	Test Conditions
T804 1400-20	2000	$T_{vj} = 125\text{ °C}$
T804 1400-22	2200	$I_{DRM} = 150\text{ mA}$
T804 1400-24	2400	$I_{RRM} = 150\text{ mA}$
		$V_{DM} = V_{DRM}, V_{RM} = V_{RRM}$
		$t_p = 10\text{ ms}$
		$V_{DSM} = V_{DRM}$
		$V_{RSM} = V_{RRM} + 100$

Outline



Current Ratings

Symb.	Parameter	Test Conditions	Min	Type	Max	Unit
$I_{T(AV)}$	Mean On-State Current	Half Sine Wave, $T_C = 70\text{ °C}$	-	-	1470	A
$I_{T(RMS)}$	RMS On-State Current	$T_C = 70\text{ °C}$	-	-	2308	A
I_{TSM}	Surge (non-repetitive) On-State Current	10ms, Half Sine Wave, $T_C = 125\text{ °C}$, $V_R = 0$	-	-	23.0	kA
I^2t	Limiting load integral	Sine Wave, 10ms	-	-	265	$10^4 A^2s$

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Characteristics

Symb.	Parameter	Test Conditions	Min	Type	Max	Unit
V_{TM}	Peak on-state voltage	$T_{vj} = 125^{\circ}\text{C}$, $I_{TM} = 3000\text{ A}$	-	-	1.65	V
I_{DRM}	Forward leakage current	$T_{vj} = 125^{\circ}\text{C}$, V_{DRM}	-	-	150	mA
I_{RRM}	Reverse leakage current	$T_{vj} = 125^{\circ}\text{C}$, V_{RRM}	-	-	150	mA
V_{TO}	Threshold voltage	$T_{vj} = 125^{\circ}\text{C}$	-	-	0.96	V
r_T	Slope resistance	$T_{vj} = 125^{\circ}\text{C}$	-	-	0.23	m Ω
I_H	Holding current	$T_{vj} = 25^{\circ}\text{C}$	-	-	200	mA
I_L	Latching current	$T_{vj} = 25^{\circ}\text{C}$	-	-	1000	mA

Dynamic Parameters

Symb.	Parameter	Test Conditions	Min	Type	Max	Unit
dv/dt	Critical rate of rise of off-state voltage	$T_{vj} = 125^{\circ}\text{C}$, $0.67V_{DRM}$	1000	-	-	V/ μs
di/dt	Critical rate of rise of on-state current	$T_{vj} = 125^{\circ}\text{C}$, $V_{DM} = 0.67V_{DRM}$, $I_{TM} = 2000\text{ A}$ $I_{FG} = 2\text{ A}$, $t_r = 0.5\text{ }\mu\text{s}$, $f = 50\text{ Hz}$	-	-	200	A/ μs
t_d	Delay time	$T_{vj} = 25^{\circ}\text{C}$, $V_{DM} = 0.5V_{DRM}$, $I_{TM} = 2000\text{ A}$ $I_{FG} = 2\text{ A}$, $t_r = 0.5\text{ }\mu\text{s}$	-	-	3.0	μs
t_q	Turn-off time	$T_{vj} = 125^{\circ}\text{C}$, $V_{DM} = 0.67V_{DRM}$, $dv/dt = 20\text{ V}/\mu\text{s}$, $V_R = 200\text{ V}$ $dI_T/dt = -10\text{ A}/\mu\text{s}$, $I_T = 2000\text{ A}$	-	300	-	μs
Q_{rr}	Recovery Charge	$T_{vj} = 125^{\circ}\text{C}$, $dI_T/dt = -10\text{ A}/\mu\text{s}$, $V_R = 200\text{ V}$, $I_T = 2000\text{ A}$	-	-	3500	μC
I_{rr}	Reverse recovery current		-	-	170	A

Gate Parameters

Symb.	Parameter	Test Conditions	Min	Type	Max	Unit
I_{GT}	Gate trigger current	$T_{vj} = 25^{\circ}\text{C}$	-	-	300	mA
V_{GT}	Gate trigger voltage	$T_{vj} = 25^{\circ}\text{C}$	-	-	3.0	V
I_{GD}	Gate non-trigger current	$T_{vj} = 125^{\circ}\text{C}$, $V_D = 0.4V_{DRM}$	10	-	-	mA
V_{GD}	Gate non-trigger voltage	$T_{vj} = 125^{\circ}\text{C}$, $V_D = 0.4V_{DRM}$	0.3	-	-	V
V_{FGM}	Peak forward gate voltage		-	-	12	V
V_{RGM}	Peak reverse gate voltage		-	-	5	V
I_{FGM}	Peak forward gate current		-	-	4	A
P_{GM}	Gate power losses		-	-	20	W
$P_{G(AV)}$	Gate power losses (mean)		-	-	4	W

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Max. on-state characteristic model

$$V_T = A + B \cdot \ln(I_T) + C \cdot I_T + D \cdot \sqrt{I_T}$$

	25 °C	125 °C
A	1.3554	1.77614
B	-0.0948075	-0.207633
C	0.0000508818	0.0000649331
D	0.0167298	0.0249235

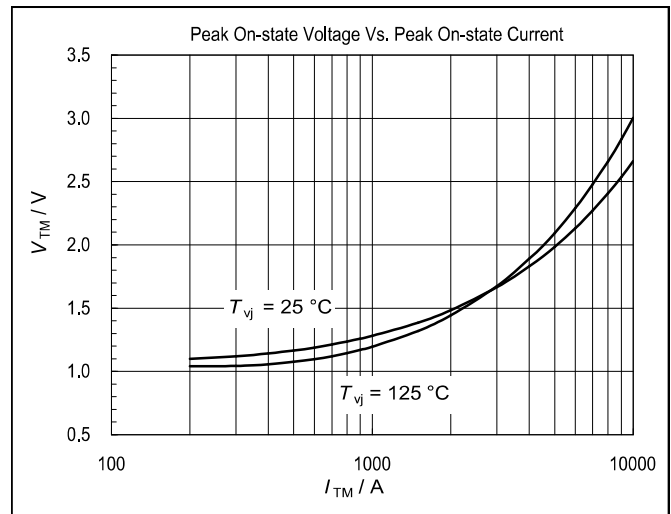


Fig1. Peak On-state Voltage Vs. Peak On-state Current

Transient thermal impedance function
(double side cooled)

$$R_{thjc}(t) = \sum_{i=1}^n R_{thi} \cdot \left(1 - e^{-\frac{t}{\tau_i}}\right)$$

i	1	2	3	4
R _{thi} (K/kW)	12.067	3.45	1.485	1.002
τ _i (s)	0.6894	0.0872	0.0217	0.0043

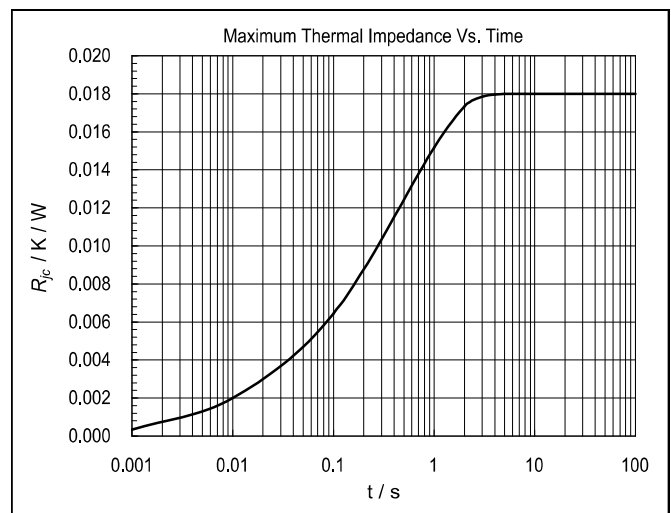


Fig2. Maximum Thermal Impedance Vs. Time

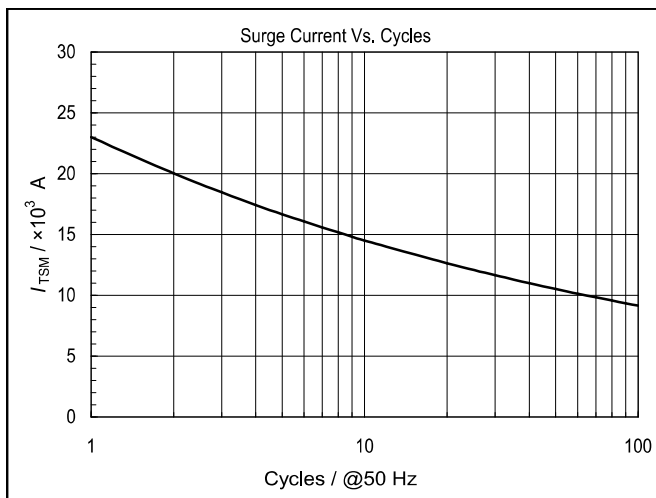


Fig3. Surge Current Vs. Cycles

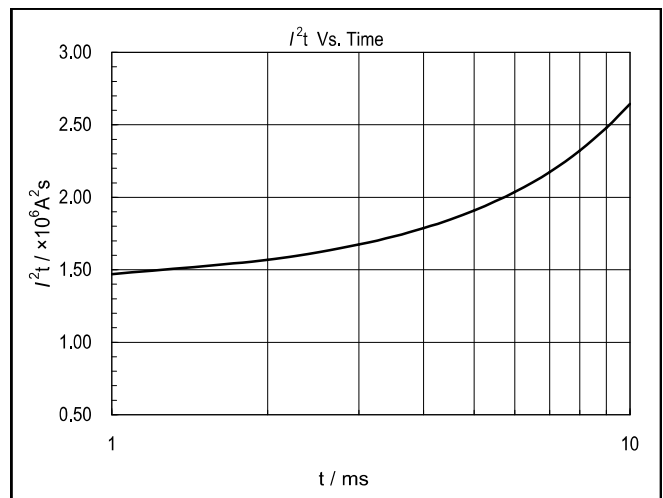


Fig4. I²t Vs. Time

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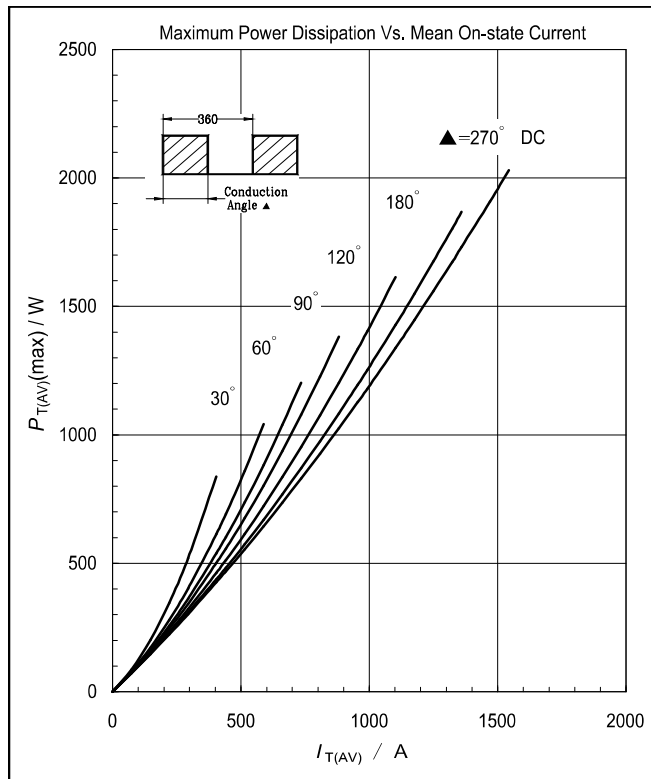


Fig5. Maximum Power Dissipation Vs. Mean On-state Current

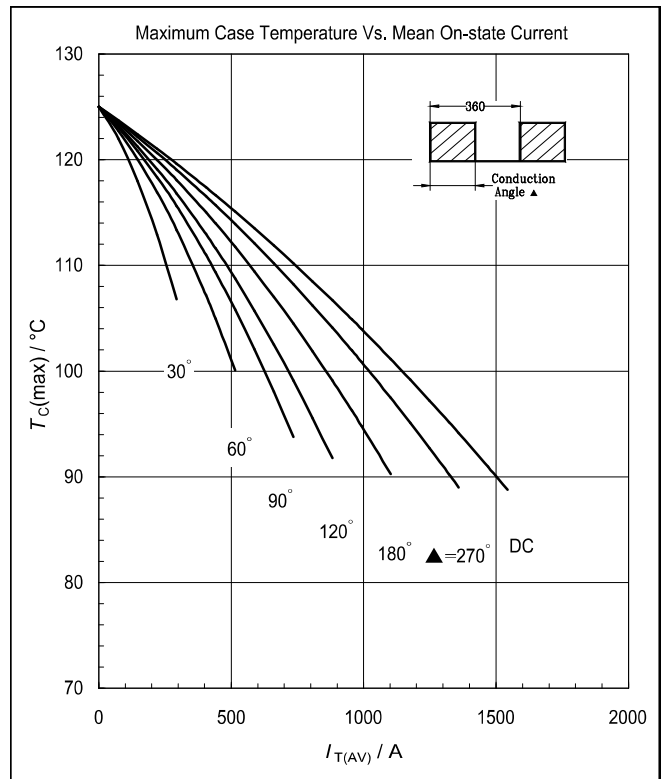


Fig6. Maximum Case Temperature Vs. Mean On-state Current

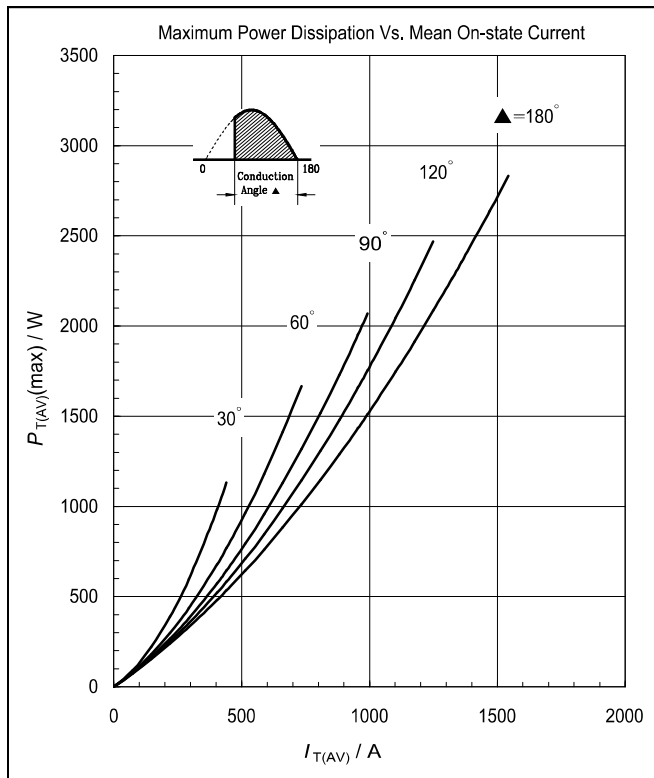


Fig7. Maximum Power Dissipation Vs. Mean On-state Current

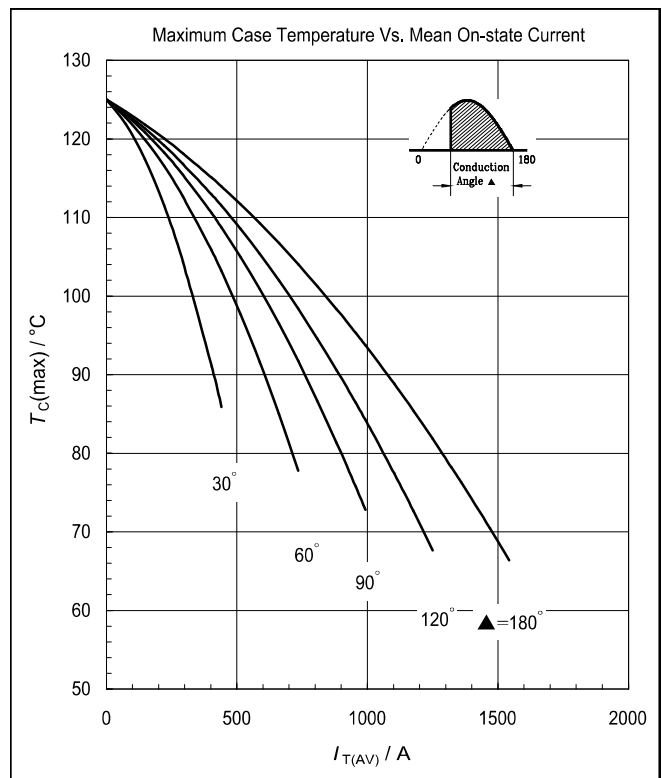


Fig8. Maximum Case Temperature Vs. Mean On-state Current

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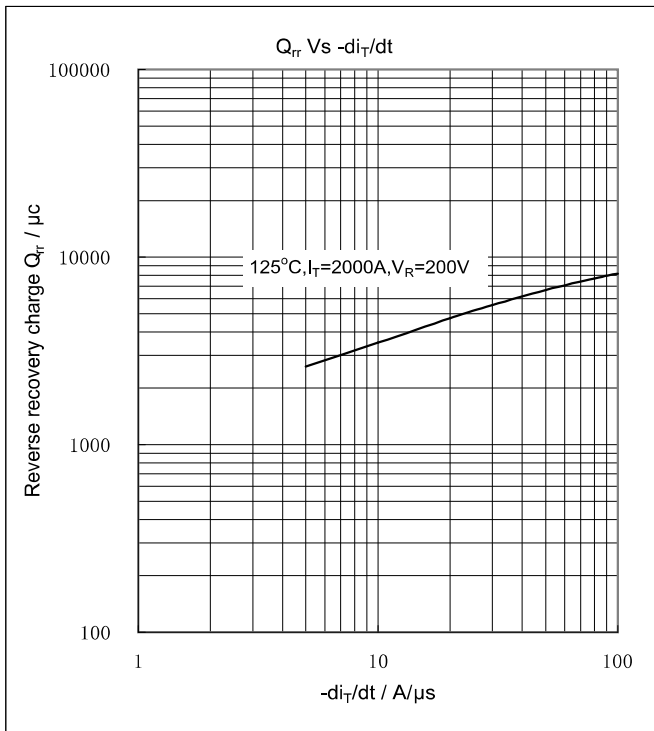


Fig9. Reverse recovery charge Vs. $-di_T/dt$

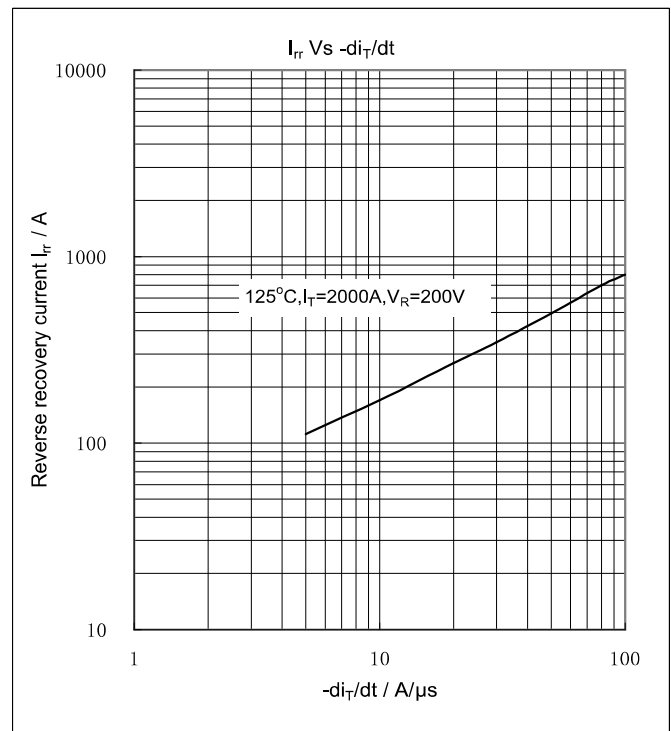


Fig10. Reverse recovery current Vs. $-di_T/dt$

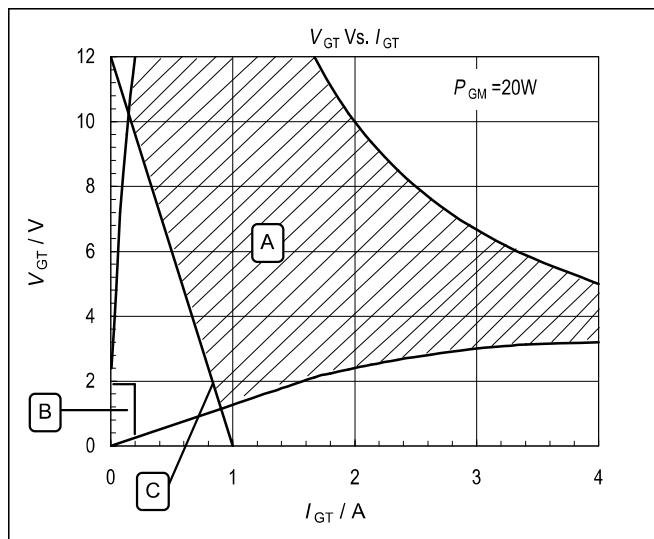


Fig11. V_{GT} Vs. I_{GT}

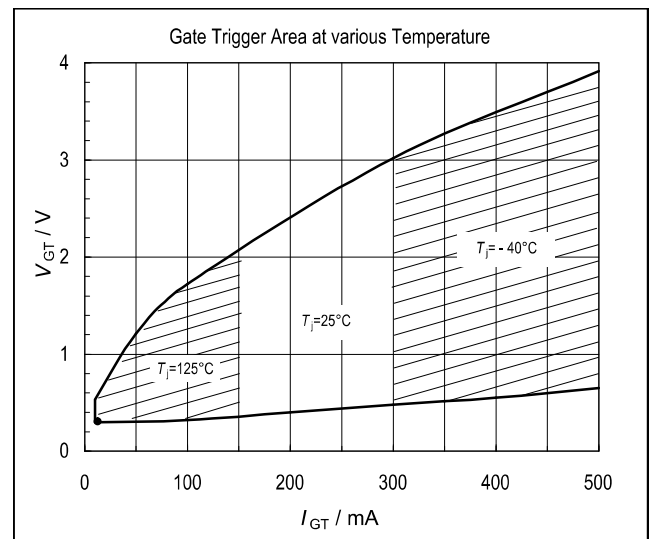


Fig12. Gate Trigger Area at various Temperature

A is Recommended Triggering Area.

B is Unreliable Triggering Area.

C is Recommended Gate Load Line.